FIG. 1

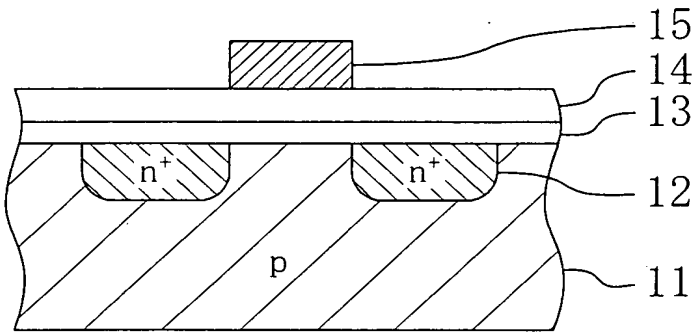
15
14
13
12
11
n+
n+
p

FIG. 2

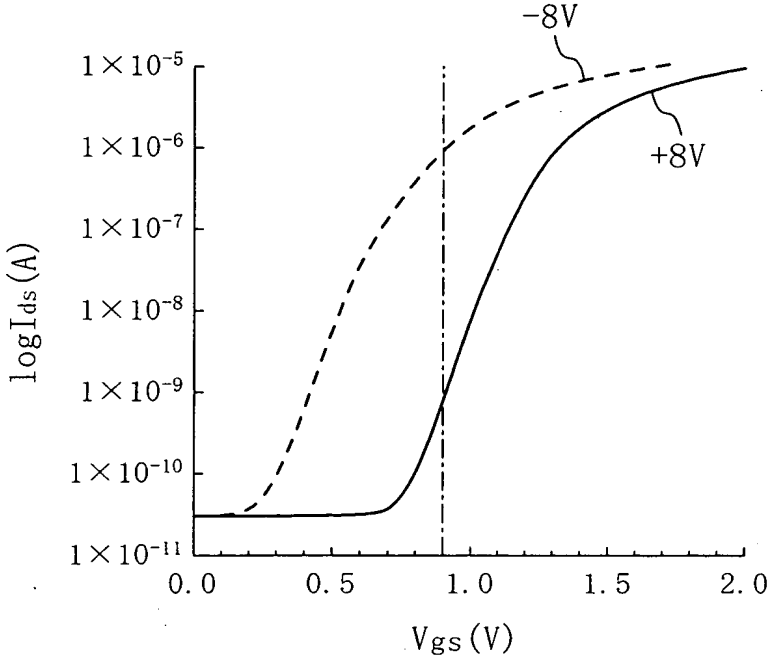
-8V
+8V
1×10-5
1×10-6
1×10-7
1×10-8
1×10-9
1×10-10
1×10-11
logIds(A)
0.0
0.5
1.0
1.5
2.0
Vgs(V)

FIG. 3

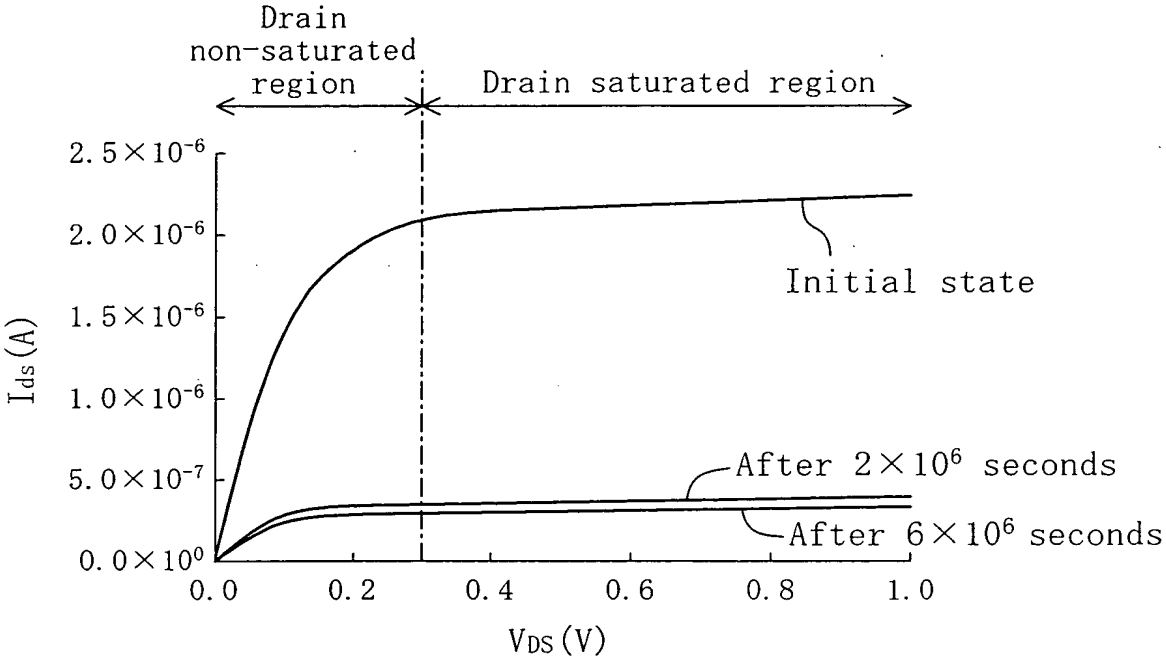
Drain non-saturated region
Drain saturated region
2.5×10⁻⁶
2.0×10⁻⁶
1.5×10⁻⁶
1.0×10⁻⁶
5.0×10⁻⁷
0.0×10⁰
Ids (A)
Initial state
After 2×10⁶ seconds
After 6×10⁶ seconds
0.0
0.2
0.4
0.6
0.8
1.0
VDS (V)

FIG. 4

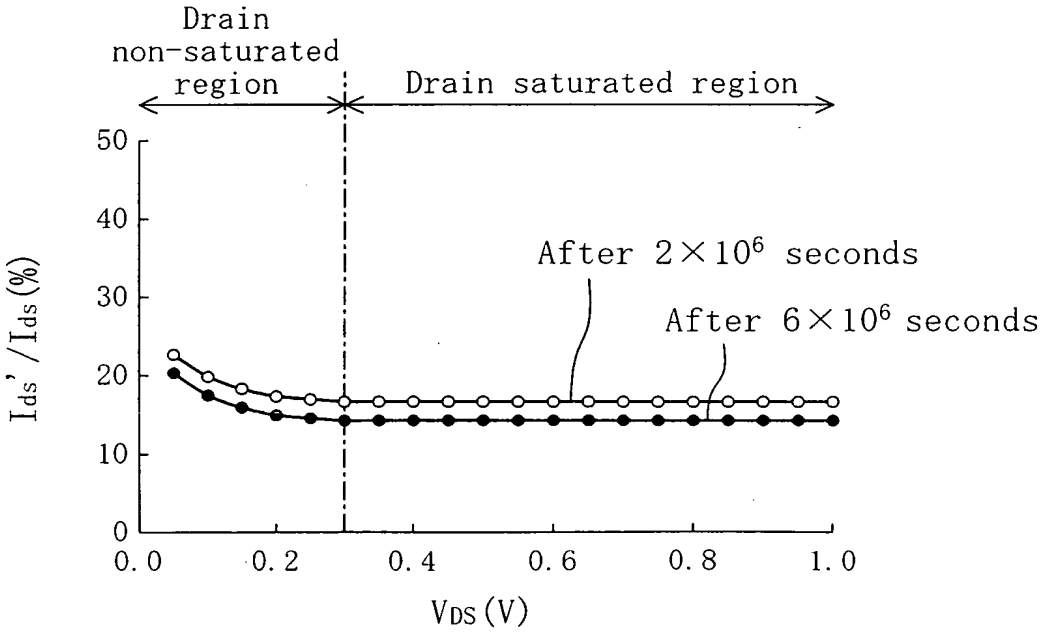
Drain non-saturated region
Drain saturated region
50
40
30
20
10
0
Ids' /Ids (%)
After 2×10⁶ seconds
After 6×10⁶ seconds
0.0
0.2
0.4
0.6
0.8
1.0
VDS (V)

FIG. 5

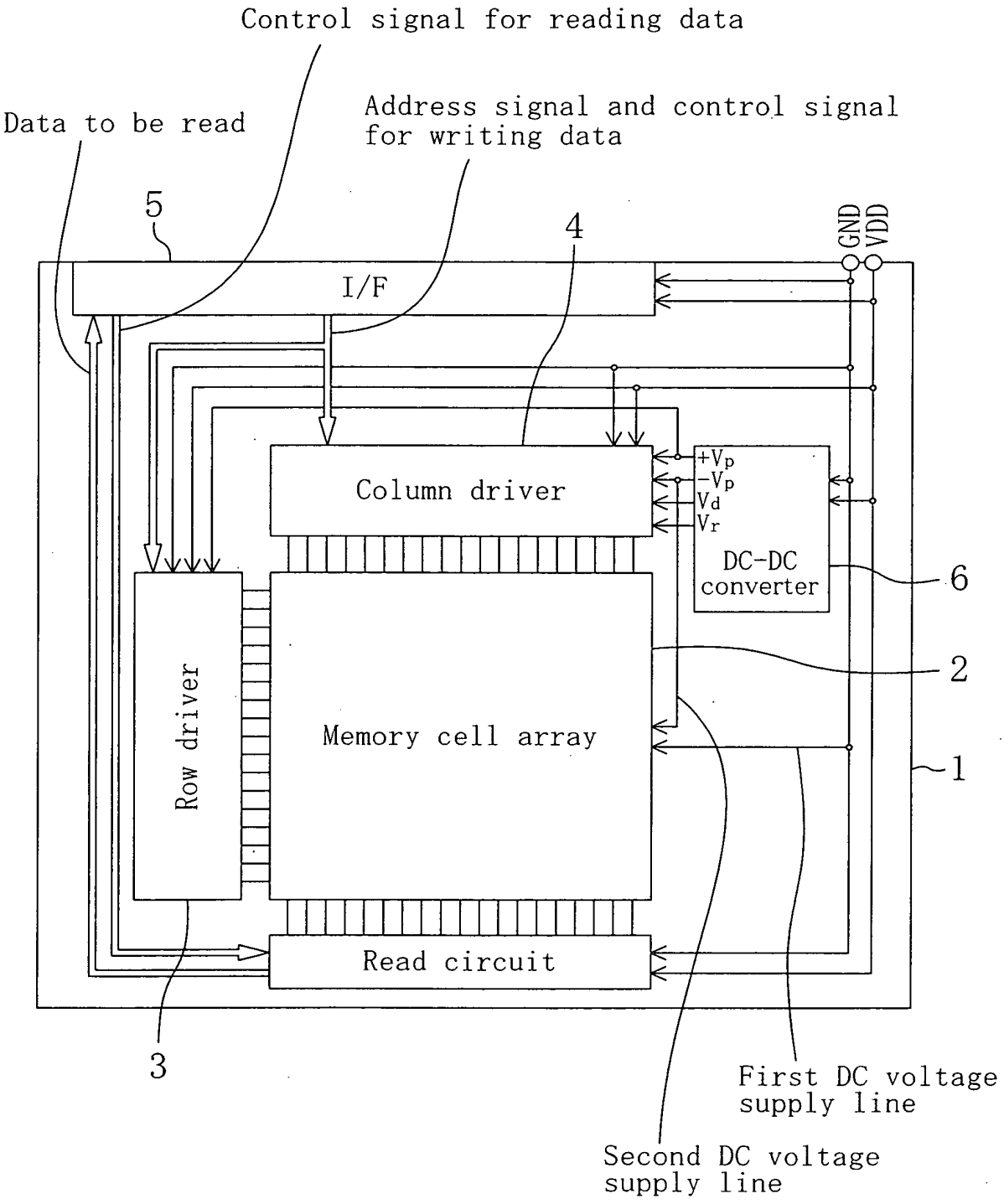
Control signal for reading data
Data to be read
Address signal and control signal for writing data
5
4
GND
VDD
I/F
Column driver
+Vp
-Vp
Vd
Vr
DC-DC converter
6
2
Row driver
Memory cell array
1
Read circuit
3
First DC voltage supply line
Second DC voltage supply line

FIG. 6
PRIOR ART

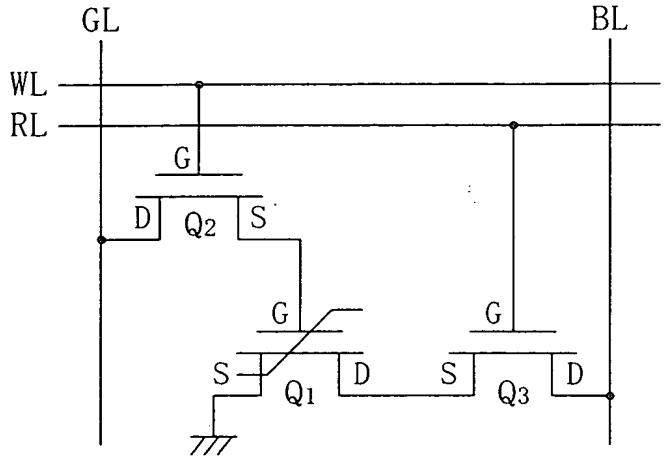

FIG. 7
PRIOR ART

	OPERATION		
	ERASE	WRITE	READ
WL	V_G	V_G	0
RL	0	0	V_G
GL	0	V_P	0
BL	0	0	V_d
SUBSTRATE	$-V_{GE}$	0	0

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